WHAT IS CLAIMED IS:

1. In a communication system, apparatus for transporting a plurality of sampled signals from a first location to a second location comprising in combination:

a source of one or more data signals and one or more clock signals at said first location;

a reference clock generating one or more reference signals at said first location;

a phase difference estimator generating a phase signal representing at least an estimate of the difference in phase between one of said clock signals and one of said reference signals;

a communication channel transmitting said one or more data signals, said one or more clock signals and said phase signal to said second location;

a resample filter located at said second location;

a selector responsive to said phase signal for conditioning the resample filter in response to said phase signal, said conditioned resample filter being responsive to said one or more data signals for generating one or more resampled data signals at the second location.

2. Apparatus, as claimed in claim 1, wherein said selector comprises a memory storing coefficients for said resample filter.

3. Apparatus, as claimed in claim 2, wherein the memory is addressed in response to said phase signal.

4. Apparatus, as claimed in claim 1, wherein said selector computes coefficients for said resample filter.

5. Apparatus, as claimed in claim 1, and further comprising a buffer at the second location for storing said one or more data signals.

6. Apparatus, as claimed in claim 5, and further comprising a second source of one or more clock signals located at the second location for clocking said one or more data signals from said buffer to said resample filter, said second source being unsynchronized with said first source.

7. Apparatus, as claimed in claim 1, wherein said data signals comprise a plurality of channels of multiplexed data signals and wherein said source comprises a demultiplexer arranged to separate said plurality of channels into individual channels and to generate one or more divided clock signals divided down from said clock signals.

8. Apparatus, as claimed in claim 7, wherein said demultiplexer extracts a frame synch signal derived from said multiplexed data signals, wherein said one or more reference signals comprise one or more coherent reference signals and wherein said phase difference estimator generates said phase signal in response to said frame synch signal, at least one of said divided clock signals and at least one of said one or more coherent reference signals.

9. Apparatus, as claimed in claim 7, wherein said one or more divided clock signals comprises a first divided clock signal having a first frequency and a second divided clock signal having a second frequency less than said first frequency and wherein said phase difference estimator generates said phase signal in response to said first and second divided clock signals and at least one of said one or more coherent reference signals.

10. Apparatus, as claimed in claim 7, and further comprising a data insertion module arranged to insert said phase signal into said plurality of channels.

11. Apparatus, as claimed in claim 1, wherein said one or more data signals further comprise frame synch signals and wherein said one or more reference signals comprise one or more coherent reference signals.

12. Apparatus, as claimed in claim 11, wherein said phase difference estimator generates said phase signal in response to at least one of said frame synch signals and at least one of said one or more coherent reference signals.

13. Apparatus, as claimed in claim 12, wherein said one or more clock signals comprise a first clock signal having a first frequency and a second clock signal having a second frequency less than said first frequency and wherein said phase difference estimator generates said phase signal in response to said first and second clock signals and at least one of said one or more coherent reference signals.

14. Apparatus, as claimed in claim 11, and further comprising a packetizing module arranged to transmit said data signals, said clock signals and said phase signal in packets.

15. Apparatus, as claimed in claim 14, wherein said one or more data signals comprises a plurality of channels of multiplexed synchronously sampled data signals and wherein said phase signal comprises a separate phase signal for each said channel.

16. In a communication system, a method of transporting a plurality of sampled signals from a first location to a second location comprising in combination:

processing one or more data signals and one or more clock signals at said first location;

generating one or more reference signals at said first location;

generating at said first location a phase signal representing at least an estimate of the difference in phase between one of said clock signals and one of said reference signals;

transmitting said one or more data signals, said one or more clock signals and said phase signal to said second location;

resample filtering said one or more data signals at said second location;

conditioning the resample filtering in response to said phase signal, said conditioned resample filtering being responsive to said one or more data signals for generating one or more resampled data signals at the second location.

17. A method, as claimed in claim 16, wherein said conditioning comprises storing coefficients for said resample filtering

18. A method, as claimed in claim 17, wherein said conditioning further comprises addressing said coefficients in response to said phase signal.

19. A method as claimed in claim 16, wherein said conditioning comprises computing coefficients for said resample filtering.

20. A method, as claimed in claim 16, wherein said transmitting comprises storing said one or more data signals at the second location.

21. A method, as claimed in claim 20, and further comprising clocking said data signals at said second location after said storing, said clocking being unsynchronized with said data clock signals at said first location.

22. A method, as claimed in claim 16, wherein said processing comprises:

processing a plurality of channels of multiplexed data signals;

dividing at least one of said clock signals into one or more divided clock signals; and

demultiplexing said plurality of channels into individual channels.

23. A method, as claimed in claim 22, and further comprising deriving a frame synch signal from said multiplexed data signals, wherein said generating one or more reference signals comprises generating one or more coherent reference signals and wherein said generating at said first location a phase signal comprises generating said phase signal in response to said frame synch signal, at least one of said divided clock signals and at least one of said one or more coherent reference signals.

24. A method, as claimed in claim 22, wherein said dividing comprises dividing said clock signals into a first divided clock signal having a first frequency and a second divided clock signal having a second frequency less than said first frequency and wherein said generating at said first location a phase signal comprises generating said phase signal in response to said first and second divided clock signals and at least one of said one or more coherent reference signals.

25. A method, as claimed in claim 22, and further comprising inserting said phase signal into said plurality of channels.

26. A method, as claimed in claim 16, wherein said processing comprises deriving a frame synch signal from said data signals, generating one or more divided clock signals derived from said clock signals and wherein said generating one or more reference signals comprises generating one or more coherent reference signals.

27. A method, as claimed in claim 26, wherein said generating at said first location a phase signal comprises generating said phase signal in response to said frame synch signal and at least one of said one or more coherent reference signals.

28. A method, as claimed in claim 26, wherein said generating one or more divided clock signals comprises generating a first divided clock signal having a first frequency and a second divided clock signal having a second frequency less than said first frequency and wherein said generating at said first location a phase signal comprises generating said phase signal in response to said first and second divided clock signals and at least one of said one or more coherent reference signals.

29. A method, as claimed in claim 26, and further comprising transmitting said data signals, said clock signals and said phase signal in packets to said second location.

30. A method, as claimed in claim 29, wherein said processing one or more data signals comprises processing a plurality of channels of multiplexed synchronously sampled data signals and wherein said generating at said first location a phase signal comprises generating a separate phase signal for each of said plurality of channels.